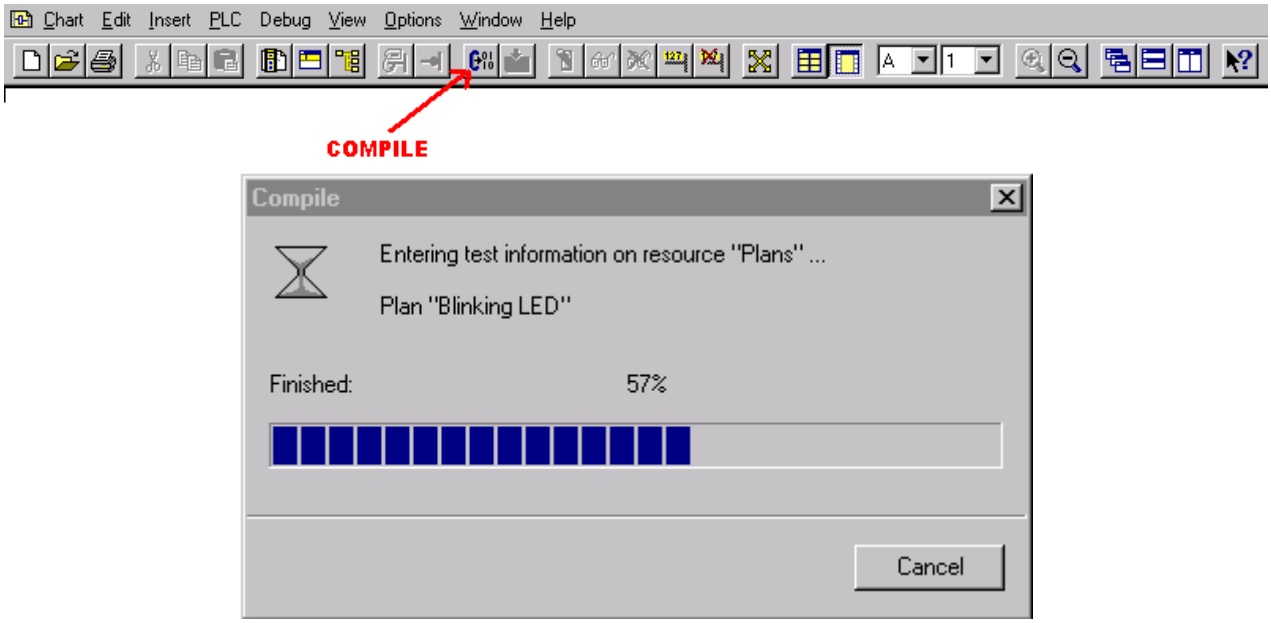
Compiling CFC charts

After positioning the gates in the CFC charts, and ensuring the correct run sequence and execution layer, the CFC-chart has to be compiled. Only once this has been completed, can the CFC logic be transferred to the device.

During the compilation the CFC-chart is compiled into executable code. Errors are automatically detected and indicated. In some cases, the compilation may also report some warnings. So for example, a warning will be indicated if there is a signal feed-back inside the CFC-chart i.e. when an input to a gate is generated by an output of a gate that is executed later in the run sequence.

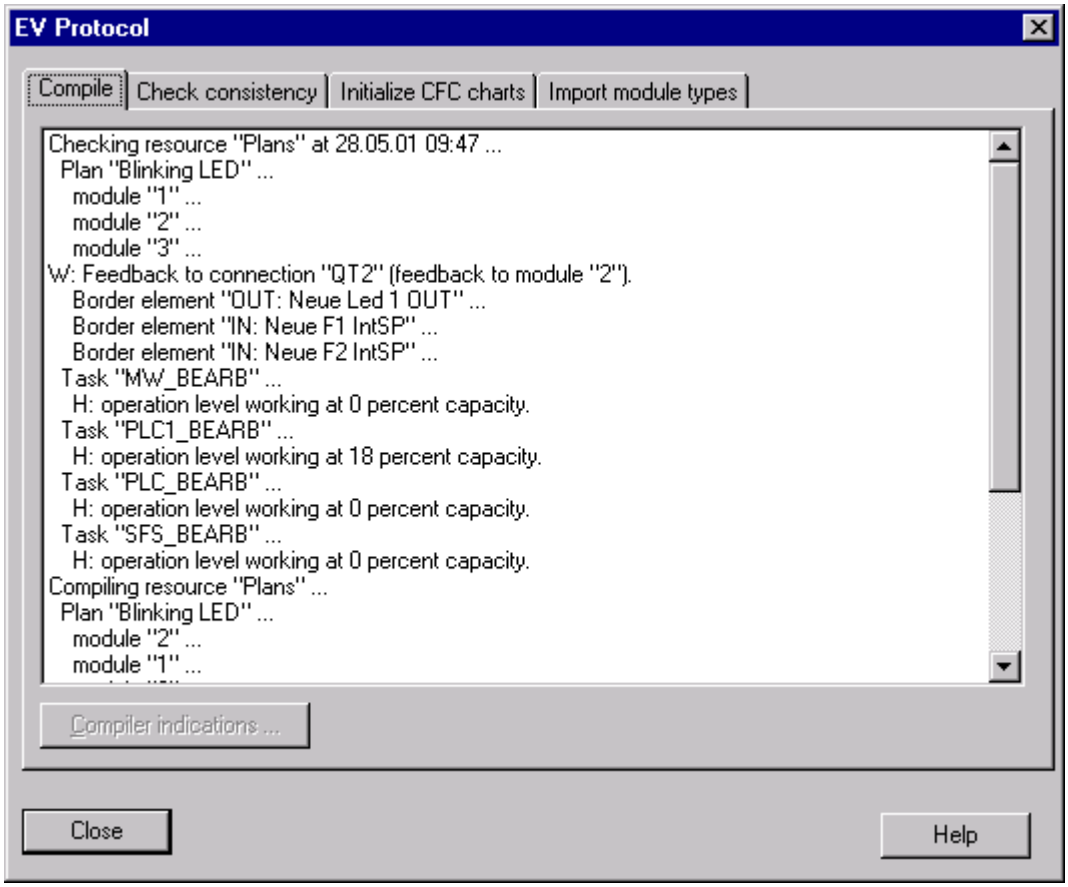


Picture 1: compiling the CFC chart

To start the compilation select “Compile” in the tool bar (see picture 2). Alternatively select Chart → Compile from the menu bar.

Initially the compilation checks syntax and capacity. If the capacity of any one of the run time groups is exceeded, an error report is generated.

If the consistency check was successful, the final report will have no errors.



Picture 2: the compilation generates a report

In the report (picture 2), errors and warnings are designated by an “F” viz a “W” at the left hand margin, followed by a plain text statement as to the nature of the error or warning. Warnings may be tolerated if the user accepts the implication. Errors however cannot be tolerated, and lead to termination of the compilation.

The restriction in the number of gates and interconnections per execution group is reflected by the resource allocation measured in so called TICKS.

In the 7SJ6 devices the following maximum number of TICKS are permitted in the various task levels:

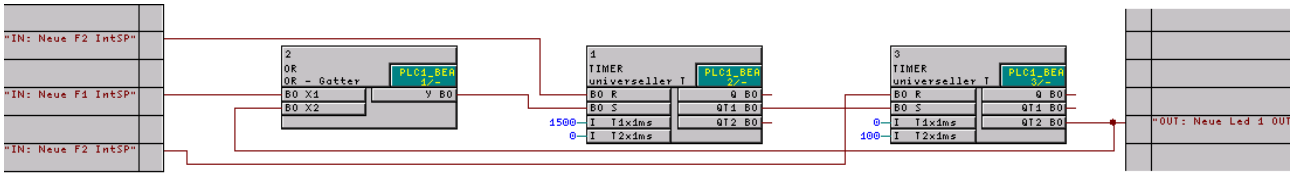
MW_BEARB :	2536
PLC1_BEARB:	255 (7SJ63 = 300)
PLC_BEARB:	130
SFS_BEARB:	2173

Resource allocation in TICKS required by the individual elements:

Individual Element	Amount of TICKS
Module, basic requirement	5
each input more than 3 inputs for generic modules	1
Connection to an input	6
Connection to an output signal	7
Additional for each configuration sheet	1

The restrictions indicated above apply to the 7SJ6 devices. They may differ in other devices.
In the event of error messages in the compilation report, these will be accompanied by statements regarding the cause of the error. In the compilation report the used capacity of each execution level is indicated in percent. In the event that a gate is placed in the wrong execution layer this will be indicated by the report.

An example of a warning message is shown below in picture 3. In this case a feedback signal is used. The feedback signal is the output from the timer gate 3 (execution sequence 3), which is connected to the input of “OR” gate number 2 (execution sequence 1).



Picture 3: Feedback signals in CFC can lead to warning messages

To avoid this warning in future, a new gate has been provided . This gate allows feedback signals within one worksheet. The function of this gate is to re-trigger the event triggered logic i.e. the run sequence will be executed again once the loop back gate detects a change of its input. The loop back gate will re-trigger the logic until its input and output have the same logic state. A maximum number of re-triggers can be entered to avoid infinite loops.