

The COUNTER module

The new COUNTER module facilitates numerous new methods for the implementation of user defined solutions via CFC logic. Hereafter an application which extends the motor protection functionality is described.

SIPROTEC 4 devices contain a start inhibit protection function within the scope of motor protection. This function utilises a thermal model which calculates an internal temperature by means of the measured currents, whereby the thermal response of the rotor modelled. Various starting characteristics are considered for this purpose. Depending on when the next starting sequence takes place in relation to the previous one, a different number of permissible starts will result based on the thermal reserve. If a starting sequence is terminated a further start may be allowed as the terminated start will not result in the same amount of heating as would have been the case for a completed starting sequence.

Some customers however insist on a strict counter which, irrespective of the starting conditions, always facilitates the same number of motor starts. The COUNTER module may be used here.

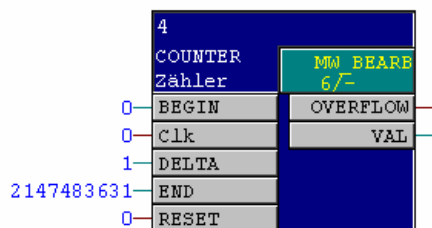


Figure 1: COUNTER

An example:

Motor starts must be detected via the binary input of a SIPROTEC device. The number of actual motor starts must be indicated as a measured value. Following the fourth motor start, an alarm must be generated to block further start initiations. This alarm must be routed to a binary output as non-latched information. Via a further binary input, the counter must be re-set.

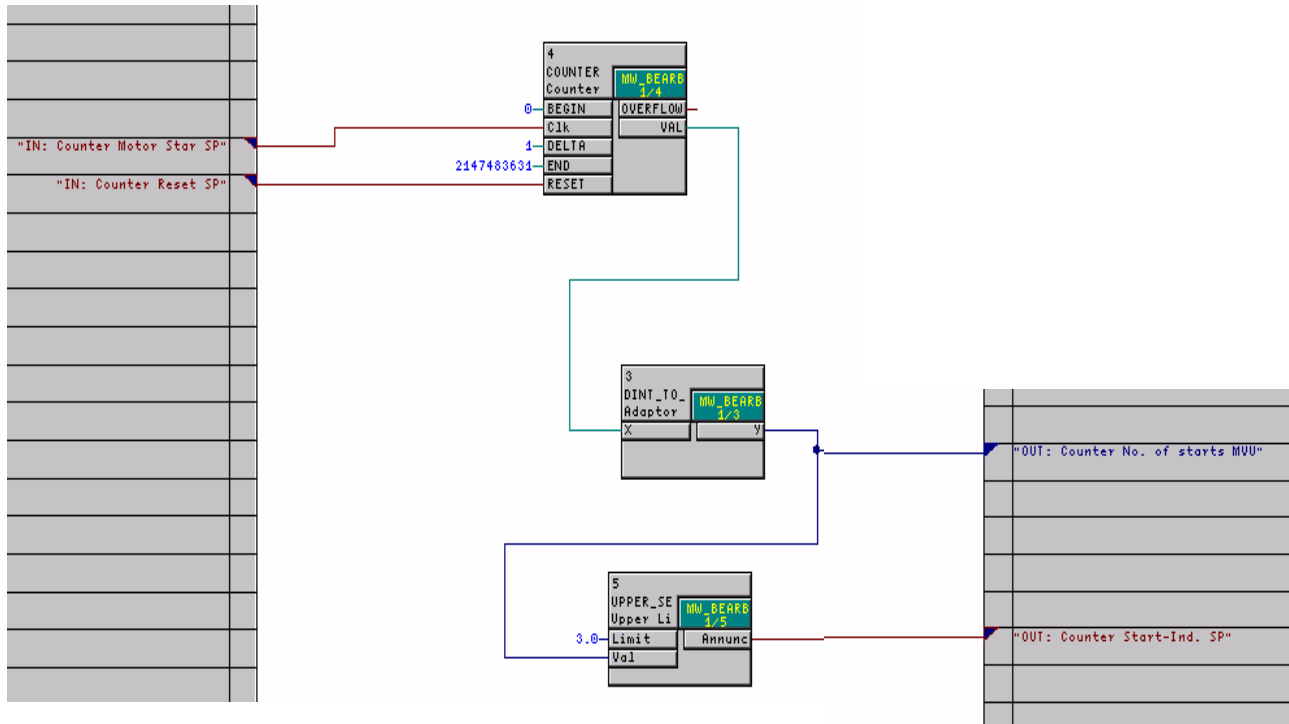


Figure 4: CFC logic

Properties of the COUNTER module:

- The Counter module counts the positive edges of the signal (clock Clk) and adds with each positive edge the value DELTA to the stored accumulated value.
- At the initial start, the counter value VAL is initiated with the amount, which is indicated at the input BEGIN.
- Following a re-start, the memorised old value stored in NVRAM is used for the counter value VAL.
- When the counter exceeds the value END, the counter state is initialised with the value at the input BEGIN, and the output OVERFLOW changes from state 0 to 1. This indicates an overflow. The signal indicating the overflow remains on until the clock input reverts to the value 0 or when the device carries out a re-start.
- By means of a rising edge at the input RE-SET the counter can explicitly be initialised with the value indicated at the input BEGIN.

I/O assignment of COUNTER

I/O assignment:

	Name	Data type	Comment	Default selection
Inputs:	BEGIN	DINT	Initial value of the counter	0
	Clk	BOOL	Counts the positive edges	0
	DELTA	DINT	Change of the metered value with positive edge at input Clk	0
	END	DINT	Final value of the counter	2147483631
	RESET	BOOL	Resets the counter to the initial value	0
Outputs:	VAL	DINT	Current status of the counter	Saved value
	OVERFLOW	BOOL	Counter overflow; indicates that the final value has been reached	0

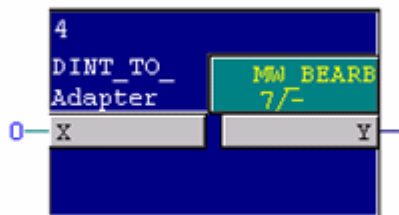
Properties of the DINT_TO_REAL module

Figure 5: DINT_TO_REAL

The **DINT_TO_REAL** block converts double integer values to real values and is thus the opposite of the **REAL_TO_DINT** block.

I/O assignment:

	Name	Data type	Comment	Default selection
Inputs:	X	DINT	Double integer input size	0
Outputs:	Y	REAL	Real output size	0.0